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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AUDUONG, GENE NGHIA	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,109	WORDEMAN ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Sywyk et al. (U.S. Pat. No. 6,262,912).

Regarding claim 1, Sywyk et al. disclose a single ended dual port memory cell memory array comprising: a plurality of single-ended, dual-port, destructive-write memory cells arranged in an array formation of rows and columns (col. 3, lines 8+; also see figures 6-7), each cell having a read port consisting of a read data terminal and a read activation terminal (figure 3, first port bitline 372, col. 3, lines 27+), and further a write port consisting of a write data terminal and a write activation terminal (figure 3, second port bitline 382, col. 3, lines 31+), the read data terminal being accessed by asserting the cell read activation terminal and the write data terminal being accessed by asserting the cell write activation terminal (read and write terminal being accessed by asserting the signals to the control gate of the access transistors), wherein in each column of cells, a read bitline connects all the read data terminals of each cell, each read bitline having a read sense amplifier connected thereto, and a write bitline with an associated write data driver connected to the write data terminal of the memory cells, and wherein when the read activation terminal is asserted, the read data terminal presents data depending upon the stored content of the memory cell, and when the write activation terminal is asserted, the content of the

memory cell is set according to the state of the write data terminal (col. 3, lines 38+; also see figures 6-7).

Regarding claims 2-3, Sywyk et al. disclose the memory array as recited in claim 1, further comprising a circuit associated with each of the read sense amplifiers and each of the write data drivers for holding data sensed by the read sensing amplifier, making data read by the read sense amplifier available to the write data driver, wherein depending on electrical signals generated outside the memory array, the circuit combines data read out from the read sense amplifier and data received from outside the memory array to make it available to the write data driver (figures 6-7; col. 3, lines 50+).

Regarding claim 4, Sywyk et al. disclose the memory array as recited in claim 1, wherein the write wordlines are coupled to the write activation terminals of the memory cells, the write wordlines being positioned orthogonally to the read and write bitlines, and wherein the plurality of read wordlines are connected to the read activation terminals of the memory cells and positioned orthogonally to the read and write bitlines (figure 3, wordlines 1 and 2 being positioned orthogonally to the read and write bitlines (bitline 1 and bitline 2)).

Regarding claim 5, Sywyk et al. disclose the memory array as recited in claim 3, wherein the read and write wordlines are asserted by a wordline decoder and by corresponding write data drivers, and wherein one read wordline and one write wordline are asserted simultaneously for different cells of the memory array (figures 6-7, read and write wordlines are asserted by wordline drivers).

Regarding claims 6-7, Sywyk et al. disclose the memory array as recited in claim 3, wherein the circuit associated with each read sense amplifier and write data driver holds data

sensed by the read sensing amplifier, providing a means for allowing data read-out of the array during one cycle to be modified and written-back to the memory array concurrently with the read-out operation of the next memory cycle, wherein the write cycle consists of read-out and write-back phases (col. 3, lines 50+).

Regarding claim 8, Sywyk et al. disclose the memory array as recited in claim 3 wherein selected bits of the data read-out are modified by input data provided from outside the memory array before being written-back during a write cycle (col. 3, lines 50+).

Regarding claim 9, Sywyk et al. disclose the memory array as recited in claim 3 further comprises an output data terminal wherein selected bits of the read-out data are outputted to outside the memory array (col. 3, lines 50+).

Regarding claim 10, Sywyk et al. disclose the memory array as recited in claim 3, wherein circuit elements connect each read sense amplifier to a corresponding write data driver to provide means for refreshing the memory cells (inherently, refreshing circuit is incorporated into the device to refresh the cells in the array to ensure the store data).

Regarding claim 11, Sywyk et al. disclose the memory array as recited in claim 3, wherein a circuit is provided with each row decoder circuit to activate corresponding write wordlines during the write-back phase of a cycle occurring concurrently with the activation of a read wordline (wordline driver).

Regarding claim 12, the memory array as recited in claim 3, wherein the write wordline circuit is a latch connected to a driver (col. 4, lines 31+).

Regarding claim 14, Sywyk et al. disclose the memory array as recited in claim 9, wherein the columns to be read out of the memory array and written into the memory array are selected by a column decoder (read column select circuit).

Regarding claim 15, Sywyk et al. disclose the memory array as recited in claim 14, wherein the column decoder activates a column read switch which connects selected read sense amplifiers to the output terminal of the memory array (write column select circuit).

Regarding claim 16, Sywyk et al. disclose the memory array as recited in claim 14, wherein the column decoder activates a column write switch connecting the memory input port to the write data drivers allowing the selected write data to override data from the read sense amplifier (col. 3, lines 50+).

Regarding claim 18, Sywyk et al. disclose the memory array as recited in claim 1, wherein the memory cells are read-out non-destructively (col. 5, lines 46+).

Regarding claim 19, Sywyk et al. disclose the memory array as recited in claim 1, wherein the memory cells are read-out destructively (col. 5, lines 46+).

Regarding claim 20, Sywyk et al. disclose the memory array as recited in claim 3, further comprising an address match detection means for detecting when a write cycle is immediately followed by a read cycle at the same address, wherein during a pipelined operation, the read cycle overlaps with a previous write cycle, and wherein when addresses of two operations coincide, input data associated with a write operation and modified by logic operations associated with the latch and the multiplexer is delivered to the memory array output data port (col. 3, lines 44+).

Regarding claim 21, Sywyk et al. the memory array as recited in claim 3, wherein the sense amplifiers are single-ended, current mode sense amplifier (col. 4, lines 7+).

Regarding claim 22, Sywyk et al. disclose the memory array as recited in claim 3, wherein the sense amplifiers are differential amplifiers (col. 4, lines 7+).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13, 17, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sywyk et al. (U.S. Pat. No. 6,262,912).

Regarding claims 13, 17 and 23, Sywyk et al. disclose the memory array having all of the limitation as recited in claim 3. Sywyk et al. fail to disclose wherein the write wordline is activated by a delayed clock and/or wherein activation of the column write switch is triggered by the delayed clock. However, it's known to one of ordinary skill in the art to understand that the memory cells in a row (word line) are activate by a row/word line activation signal, in which based on the timing interval (delayed of time) which is counting by the clocking in the device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sywyk's teaching to include limitation wordline is activated according the clock signal and it's delaying in a predetermined delayed of time interval to ensure the data to be stored or read-out.

Regarding claim 24, Sywyk et al. disclose the memory array having all of the limitation as recited in claim 3 but fail to disclose wherein the memory cells are selected from the group of cells consisting of 3-transistors and l-capacitor (3T 1C); z-transistors and 1-capacitor (2T 1C); and l-transistor and l-capacitor (1T 1C). The type of memory cell to be used in the device can be selected from the list of known and conventionally used (also see the description of Applicant Admitted Prior Art figures 2-3) and it's a matter that can be decided at the discretion of a person skill in the art.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
April 6, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818